MBQ-003-0027804 Seat No. _____

M. Sc. (ECI) (Sem. VIII) (CBCS) Examination

April / May - 2018

Fundamentals & Practice : Paper-32 – VHDL

(New Course)

Faculty Code : 003
Subject Code : 0027804

Time : $2\frac{1}{2}$ Hours] [Total Marks : **70**

Instructions :

(1) All questions carry equal marks.

(2) Figures on right hand side indicate marks.

1 Answer the following : (Any **seven**) **14**

1. Write a full form of VHDL and the application of VHDL.
2. What is EDA tool ?
3. Write the fundamental units of VHDL.
4. Write about the 8-valued logic system of VHIDL.
5. Write the syntax of user defined data types of VHDL.
6. Make a list of all logical operators used in VHDL.
7. What is operator overloading in VHDL ?
8. Write a syntax of GENERIC statement of VHDL code.
9. What is concurrent code in VHDL ?
10. What is the function of guarded block statement in VHDL code ?

2 Answer the following : (Any **two**) **14**

1. Write about Pre-Defined data types of VHDL. **7**
2. Write a VHDL code for D-Flip Flop. **7**
3. Write a VHDL code for vector shifter. **7**

3 Answer the following : 14

1. Write a note on Data Attributes and Signal Attributes of VHDL. 7

2. Write a note on combinational versus sequential logic of VHDL. 7

OR

3 Answer the following : 14

1. Write a brief note on Assignment, Logical and Shift operators of VHDL. 7

2. Write a VHDL code for generic parity detector, according to the top level diagram shown in the fig. (1). 7

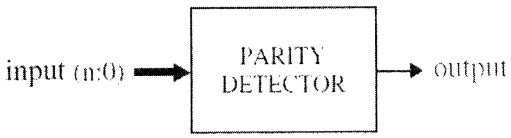

Fig. (1)

4 Answer the following : 14

1. Write a VHDL program for Multiplexer, according to the top-level diagram shown in Fig. (2). 7

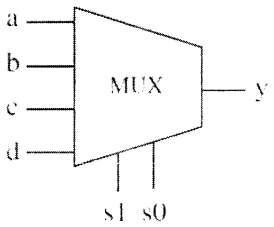

Fig. (2)

2. Write a note on LOOP and WAIT statements of VHDL. 7

5 Answer the following : (Any **two**) 14

1. Write a VHDL program for ROM. 7

2. Write a VHDL program for 10–digit BCD counter using Finite State Machine approach. 7

3. Explain Signed and Unsigned comparator with examples. 7

4. Write a note on Mealy State Machine. 7